8.1 An 8Gb/s/pin 9.6ns Row-Cycle 288Mb Deca-Data Rate SDRAM with an I/O Error-Detection Scheme

Kyu-hyoun Kim, Uksong Kang, Hoe-Ju Chung, Duk-Ha Park, Woo-Seop Kim, Young-Chan Jang, Moonsook Park, Hoon Lee, Jin-Young Kim, Jung Sunwoo, Hwan-Wook Park, Hyun-Kyung Kim, Su-Jin Chung, Jae-Kwan Kim, Hyung-Seuk Kim, Kee-Won Kwon, Young-Taek Lee, Joo Sun Choi, Changhyun Kim

Samsung Electronics, Hwasung, Korea

There is an increasing demand in the market for a high-density high-speed memory for high-end servers and network applications. This demand drives the need for development of high-performance high-density memory devices with cost-effective ways including the use of a conventional DRAM process. The main requirements for such devices can be summarized as high data bandwidth and fast random-access cycle. Because the timing budget is very marginal at extremely fast I/O speed, the probability of bit-error occurrence in I/O is remarkably high. For a fault-tolerant system that detects occasional I/O errors, an area-efficient error-detection code such as CRC is required. Such redundant information may be transferred either by adding extra pins to the bus or by adding extra bits to the burst length. Since adding an extra pin has cost implications, increasing the burst length is preferred. However, this makes the burst length a number that is not a power of 2 (i.e., 2, 4, 8…) anymore. Hence, the bursting time of such a burst length is not a multiple of the clock period as shown in Fig. 8.1.1(a), where the performance would be degraded due to the timing bubble. The performance loss is further increased as the ratio of data rate over clock frequency increases. In this paper, a deca-data rate (DecDR) scheme is proposed, where 10b are serially transferred during one clock cycle in order to have inherently compatibility with 8:2 or 16:4 CRC. Proposed DecDR scheme could be also used for other purposes such as 8b/10b coding and core ECC bit transfer.

An area-efficient $6F^2$ folded-BL twin cell (rather than $8F^2$ twin cell [1]) is adopted for the fast row cycle. The twin cell is immune to inter-BL differential noise imbalance resident in the conventional $6F^2$ open-BL sensing scheme [2]. Moreover, intra-BL coupling is also relaxed compared to $8F^2$ cell due to its 1.5-times wider BL pitch. The results are compared to a conventional design that is implemented with an identical technology as a reference. The twin-cell scheme can reduce tRAS by 7.4ns, because the restore time is no longer limited by data 'high' by virtue of its complementary nature. WL risetimes are improved by subdividing the array to have 64b (128cell)/WL. This reduces t_{RAS} and t_{RP} by 4.6ns and 3.2ns, respectively. A direct sense amplifier is adopted to minimize t_{RCD}, t_{RAC} and reduce t_{RC} by 2ns for ACT-READ-PRE cycle. In summary, the final row cycle time (t_{RC}) of 9.6ns can be achieved at a V_{DD} of 1.6V. DRAM core schemes and performances are summarized in Fig. 8.1.2.

Penta-phase clocking scheme is proposed to implement DecDR with reduced clock power and logic complexity. As shown in Fig. 8.1.3, there are two alternative methods to implement DecDR of 8Gb/s. One is to use 2GHz quad-phase clocks and the other is to use 1.6GHz penta-phase clocks. Because the 2GHz I/O clock frequency is not a multiple of the 800MHz external clock frequency in the quad-phase scheme, it is difficult to implement the pipeline (or serializer between the core and the transmitter). Besides, the relationship between I/O clock and the external clock should be properly selected and matched by some learning procedures during initialization, so that a memory controller could decide at which clock edge it can issue a command, because those two clocks would be aligned every other external clock edges. However, the command-bus efficiency becomes poor due to the restriction. Moreover, the penta-phase clock distribution power is slightly less than quad-phase due to the use of lower clock frequency in spite of the additional number of clock lines.

16:4 CRC is used as an error detection code. Although byte-wide 8:2 CRC can be used, but 16:4 CRC is more advantageous in terms of code-calculation timing budget and error-detection coverage. The CRC generator and checker are implemented using combinational logic instead of LFSR and have a maximum of 4 XOR-gate delay (around 1ns). The CRC generation and checking is separated for each lane in order to be able to identify at which lane the error is detected. For that matter, CRC results for each lane are temporally stored in an internal register that can be accessed by the memory controller to identify the defective lane after the negative acknowledge (NAK) signal is activated when at least one lane reports CRC error.

Figure 8.1.4 shows key I/O circuits for DecDR. Penta-phase PLL is based on an interpolative oscillator [3, 4, 5]. Its oscillation frequency is faster than that of conventional 3-stage ring oscillator. Moreover, it has better jitter performance than 3-stage ring oscillator, since the signal passes through higher number of gates during shorter time resulting in further averaging out of high-frequency noise. For the VCO operation, the supply voltage of the ring oscillator is generated from a variable voltage regulation amplifier. This regulation reduces jitter to acceptable limits for 8Gb/s operation. A direct interpolating inverter oscillator as in [3, 4] with fixed interpolation ratio is chosen, because it has almost twice the frequency with almost half the power consumption of those of weight-controlled pseudo NMOS stage [5]. It also has more linear gain over the same frequency range to produce smaller jitter. Since penta-phase has an odd number of clocks, no two phases can ever be differential with respect to each other. Therefore, an inverter is used to generate the complementary clock of each phase for mixed clock-data pulse generation in the 5:1 multiplexer. This inverter delay raises the crossing-point voltage between pulses to guarantee that the current source of the differential muti-input OR gate is operating in its saturation region, which consequently results in better eye opening. On the other hand, the penta-phase clocking scheme is inherently robust against duty-cycle error of individual clock signals, since it only utilizes rising edges of each clock phase.

In Fig. 8.1.5, the simulation results show a comparison of 3 different alternatives of CRC configurations. It can be seen that CRC drastically improves fault-tolerance performance of a system with failure probability enhancement of several decades depending on the BER. 16:4 CRC detects 1b error 100% within 20b and up to 3b errors with higher than 90% coverage whereas the other two alternatives oguarantee only 1b error reliably.

Several DFT features are proposed and adopted in the chip design to characterize high-speed I/O and core performances separately, and in order to utilize low-speed ATE. One of the DFT features is 2-chip loop-back testing using PRBS and inherent CRC for realistic I/O-performance verification. Another interesting DFT feature is a 2-chip transparent mode where data is written in parallel at low speed and then serially read back through 1-pin at normal speed in the TX chip, and vice versa in the RX chip.

The chip is fabricated using an 80nm DRAM process. Figure 8.1.6 shows the Shmoo plot of t_{RC}, tested using low-speed I/O access mode, in an ATE. The plot shows that a t_{RC} of 9.6ns is achieved at a V_{DD} of 1.6V. Measurements confirm an I/O operation of up to 9Gb/s at a V_{DD} of 1.8V. The eye diagram is characterized using a combination of an ATE (Agilent-93000), a parallel BER tester (ParBERT), and a real-time oscilloscope. About 0.77UI eye opening is achieved at 8Gb/s using a 70cm SMP cable with ~12GHz bandwidth.

References:

[1] H. Noda, et al., "A 4.8-ns Random Access 144-Mb Twin-Cell-Memory Fabricated using 0.11-μm Cost-Effective DRAM Technology," *Symp. on VLSI Circuits*, pp. 188-189, June, 2004.

[2] T. Takahashi, et al., "A Multi-Gigabit DRAM Technology with $6F^2$ Open-Bit-Line Cell Distributed Over-Driven Sensing and Stacked-Flash Fuse," *ISSCC Dig. Tech. Papers*, pp. 380-381, Feb., 2001.

[3] K-h. Kim, et al., "A 20GB/s 256Mb DRAM with an Inductorless Quadrature PLL and a Cascaded Pre-emphasis Transmitter," *ISSCC Dig. Tech. Papers*, pp. 470-471, Feb., 2005.

[4] K-h. Kim, "Hyper-ring oscillator," US patent, US 2005/0057316 A1, Mar., 2005.

[5] F. H. Gebara, J. D. Schaub, A. J. Drake, K. J. Nowka, and R. B. Brown, "4.0GHz 0.18μm CMOS PLL Based on an Interpolative Oscillator," *Symp. VLSI Circuits*, pp. 100-103, June, 2005.

 1-4244-0079-1/06/$20.00

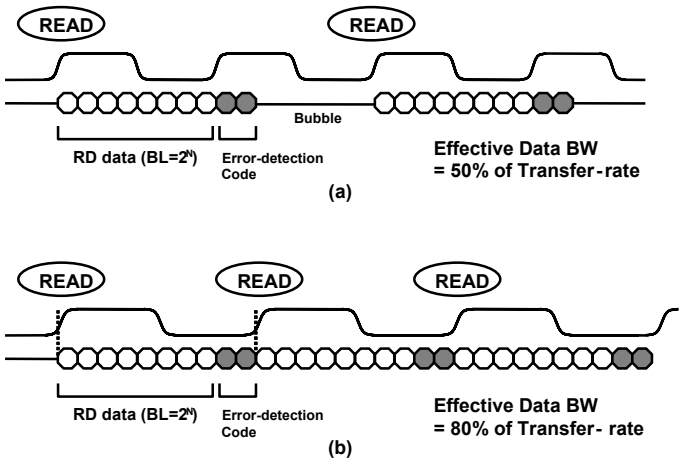
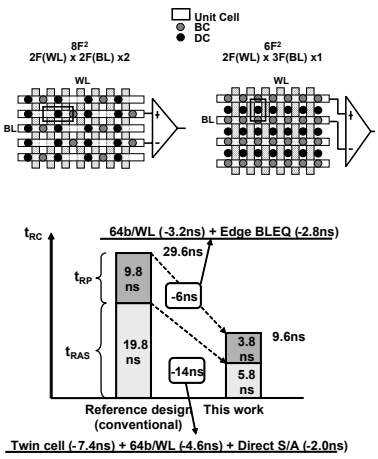


Figure 8.1.1: Timings of DRAM with error-detection code.



Chip Summary	
Density	288Mb (32MbX9)
Process	80nm 3-Al, 1-W, dual-oxide dual-poly DRAM process
Cell	6F² Twin cell (12F²)
Sub-array	256cell/BL x 64b(64 twin-cell)/WL
Architecture	8 banks, 2.3kB page size 144b prefetch
Power supply	1.8V / 1.2V (VDDIO)
Core ac Parameters (Room Temp)	$t_{AA}/t_{RCD}/t_{RP}$ =6ns/2ns/3.8ns
	t_{RRD}/t_{CCD} =2ns/2ns
	t_{RC}=9.6ns
I/O	LVDS, uni-directional DQ
PLL Jitter	14ps
Data rate	8Gb/s/pin (including CRC)
Peak BW	6.4GB/s/chip (data only)
Chip Size	6.64mm x 13.86mm
PKG	104 ball FBGA
Power	3.9W (worst-case)

Figure 8.1.2: DRAM core scheme.

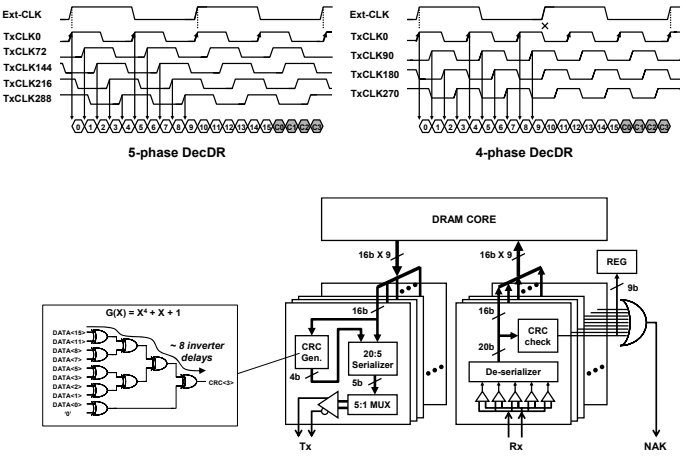


Figure 8.1.3: Timing and block diagram of data path.

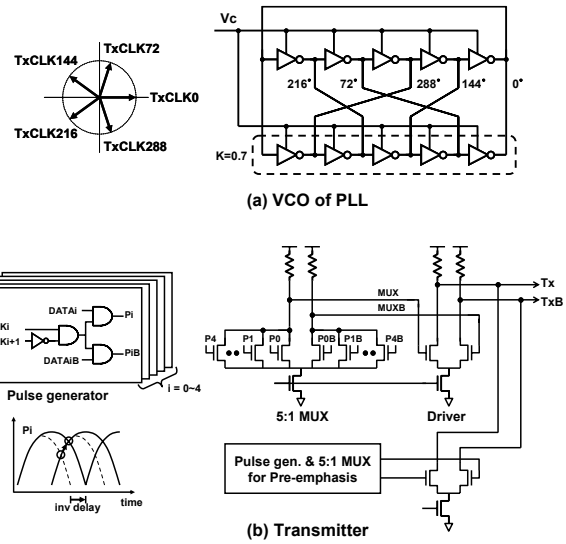
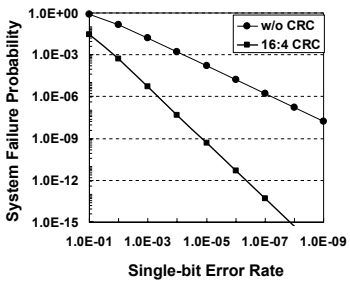


Figure 8.1.4: Key I/O circuits.



No. of errors per frame [bits]	Error detection coverage [%]		
	16:4 CRC	8:2 CRC	16:2 CRC
1	100	100	100
2	97.4	73.3	70.6
3	90.3	43.3	44.1
4	83.6	21.4	44.1
5	77.5	0.0	0.0
Max. burst error bits	> 10b	2b	2b

Figure 8.1.5: Error-detection performance (simulated).

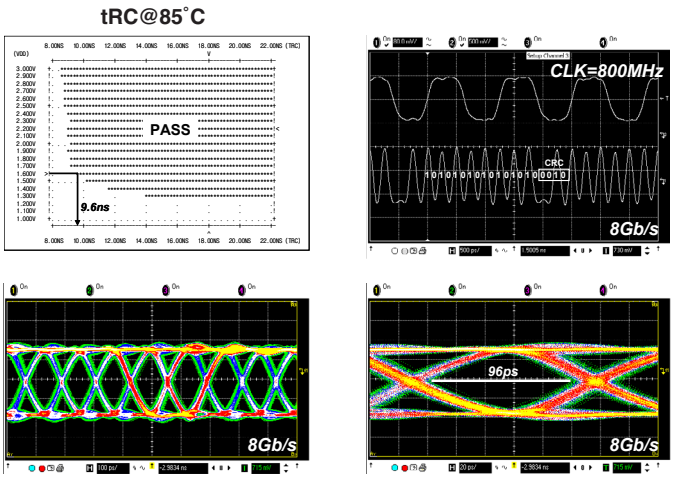


Figure 8.1.6: Measurement data.

Continued on Page 645

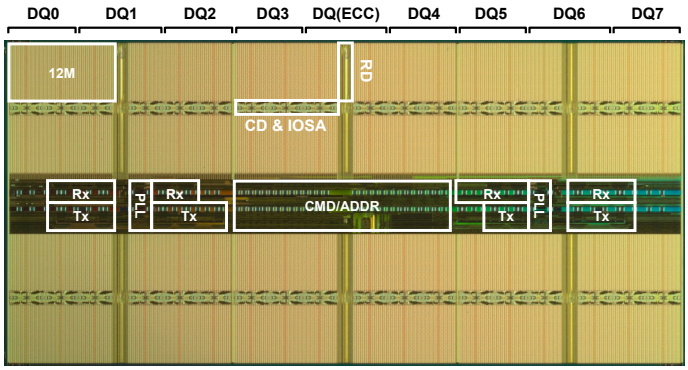


Figure 8.1.7: Die micrograph.

